Call for Papers --- IEEE CAS-FEST 2010

December 12, 2010
Athens, Greece

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CAS-FEST 2010 Topic: VARIATION-AWARE DESIGN FOR NANOSCALE VLSI CIRCUITS

Nanometer-scale CMOS technologies are plagued by significant variations and these are projected to grow more critical in the coming years. Variability is steadily eating into design margins and yield, so that mainstream current-day methodologies will be unsustainable in the future. These variations may arise from fluctuations attributed to the manufacturing process (e.g., drifts in channel length, oxide thickness, threshold voltage, or doping concentration), which affect the circuit yield, as well as variations in the environmental operating conditions (e.g., supply voltage or temperature), or due to reliability-driven circuit aging during the life of the chip. These effects can cause unacceptable alterations in circuit performance parameters, and reliable variation-tolerant design is imperative. These variations affect analog as well as digital circuits, and new design techniques and methodologies must be developed in all domains.

A number of potential approaches are available for overcoming these effects, ranging from presilicon design to postsilicon fixes, designed to make integrated circuits resilient to variations, and this field remains an area of active research today. Ingredients of variation-aware solutions include new analysis techniques, novel hardware approaches, and new optimizations. Solutions must envelop all layers of design abstraction, from the system level to the device level, and cross-layer optimizations must be developed to ensure appropriate handoff within a design flow.

The goal of CAS-FEST is to bring together the research community in this area under a single roof for an exposition of state-of-the-art techniques, nascent research, and future directions in this field, promoting a better understanding and improved cross-fertilization of ideas.

TOPICS

Topics covered by the meeting include, but are not limited to:

- Modeling and simulation in the presence of on-chip variability
- Variation-aware circuit synthesis
- Statistical timing and power analysis
- Digitally assisted/enhanced analog circuits
- Reliability issues in nanoscale circuits
- Power grid analysis and optimization
- Thermally-aware design
- Soft errors and radiation hardening
- Layout issues in design for manufacturability
- Fault tolerance and dependability
- Variation-tolerant analog circuit design
- Test issues in the presence of variation
- Resilient circuits

IMPORTANT DATES

Paper Submission	September 30, 2010
Notification of acceptance	November 1, 2010
Meeting	December 12, 2010

ORGANIZING COMMITTEE

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