Finland Section SP / CAS Chapter

- in collaboration with-

SoC 2013

The International Symposium on System-on-Chip

Tampere, Finland *October 23-24, 2013*

Organizer: *Tampere Univ. of Tech*

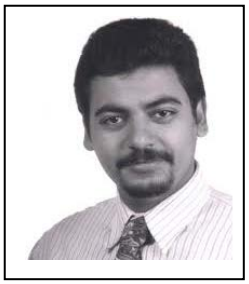
Technical co-sponsor: *IEEE Circuits and Systems Society*

A treat for IEEE members at the 15th International Symposium on System on Chip (SoC 2013)!

The International Symposium on System on Chip, co-sponsored by the IEEE CASS, is one of the premier scientific conferences on SoC, NoC, and other Embedded System technologies within the North European Region. This year, SoC 2013 has agreed to allow free access to the entire tutorial day (22nd October) and also to the keynote speeches (23rd & 24th October) to members of IEEE in Finland. Invited speakers include, but not limited to Prof. Yehea Ismail and Dr. Rajiv Joshi, both of whom are Distinguished Lecturers at the IEEE CAS Society. This event is co-arranged by the Tampere University of Technology and the IEEE Signal Processing and Circuits and Systems Joint Chapter of the Finland Section. Information about registration and other practicalities will be available on the Chapter website and LinkedIn group later in September. So, stay tuned!

Tampere – The SoC City!

List of Speakers



Prof. Yehea Ismail is an IEEE Fellow and the Director of the Center of Nanoelectronics and Devices (CND), Zewail City and American University at Cairo. He is a Distinguished Lecturer of IEEE CASS for the years 2012-2013. Previously, he was the director of the Nanoelectronics Integrated Systems Center (NISC) at Northwestern University. He is the Editor-in-Chief of the IEEE Transaction on VLSI (TVLSI) and has several awards such as the USA National Science Foundation Career award, the IEEE CAS outstanding author award, many best paper awards and teaching awards. Professor Ismail has published more than 150 papers in the top refereed journals and conferences and has coauthored few books and book chapters and many patents. His work is some of the most highly cited in the VLSI area.

Dr. Rajiv V. Joshi is a research staff member at T. J. Watson research center, IBM. He received his B.Tech degree from Indian Institute of Technology (Bombay, India), M.S degree from Massachusettes Institute of Technology and Doctorate in Eng. Science from Columbia University, USA. His novel interconnects processes and structures for aluminum, tungsten and copper technologies which are widely used in IBM for various technologies from sub-0.5µm to14nm. He has expertise in technology, circuit design, CAD, and predictive techniques and interest in predictive analytics. He received 3 Outstanding Technical Achievement (OTAs), 3 Corporate Patent Portfolio awards for licensing contributions, holds 54 invention plateaus and has over 185 US patents and over 350 including international patents. He has led successfully pervasive statistical methodology for yield prediction and also the technology-driven SRAM at IBM Server Group. He commercialized these techniques. He is a recipient of 2013 IEEE CAS Industrial Pioneer Award. He is IEEE and ISQED fellow and distinguished alumnus of IIT Bombay. He serves as an Associate Editor of TVLSI. He served on committees of ISLPED (Int. Symposium Low Power Electronic Design), IEEE VLSI design, IEEE CICC, IEEE Int. SOI conf ISQED and Advanced Metallization Program committees. He is SRC liaison with universities.

Prof. Roberto Giorgi is an Associate Professor at Department of Information Engineering, University of Siena, Italy. He was Research Associate at the University of Alabama in Huntsville, USA. He received his PhD in Computer Engineering and his Master in Electronics Engineering, Magna cum Laude both from University of Pisa, Italy. He is the coordinator of the European Project TERAFLUX in the area of Future and Emerging Technologies for Teradevice Computing. He is participating in the European projects HiPEAC (High Performance Embedded-system Architecture and Compiler), ERA (Embedded Reconfigurable Architectures). He contributed to SARC (Scalable ARChitectures), ChARM (performance evaluation of ARM-processor based embedded systems). His current interests include Computer Architecture themes such as Embedded Systems, Multiprocessors, Memory System Performance, Workload Characterization.

Dr. Tapani Ahonen is a Research Fellow at Tampere University of Technology (TUT) in Tampere, Finland, where he has held various positions since 2000. Since 2004 he is co-managing a large research group together with Professor Jari Nurmi. He is a part-time Senior Scientist at Technoconsult ApS, Denmark, where his duties include scientific coordination of an ARTEMIS project involving 26 participant organizations from ten different countries. He is also a part-time Lecturer (Nebenberuflicher Lektor) at Carinthia Tech Institute (CTI) - University of Applied Sciences in Villach, Austria since 2007. In 2009-2010 Ahonen was a Visiting Researcher (Chercheur InvitÃ©) at UniversitÃ© Libre de Bruxelles (ULB) in Bruxelles, Belgium. His work is focused on proof-of-concept driven computer systems design with emphasis on many-core processing environments. Ahonen has an MSc in Electrical Engineering and a PhD in Information Technology from TUT. Recent professional activities and service of Dr. Ahonen include active European project preparation and conference organization.

Tutorial Title: Many-Core Chips: The New High-Performance Computing Platform

Scaling as we know it is taking a different direction from the last three decades. Chips with tens of billions of transistors and hundreds of cores are expected to be the future of scaling. These chips will achieve performance through parallelism and application specific optimized cores. This trend will use superior technologies to integrate more cores on a chip rather than to push the frequency envelope as in the past. It is expected that every aspect of design and analysis will need to be modified to accommodate this new platform and trend. There is a clear need for new CAD tools and design methodologies that are very different from existing tools in both their focus and scope. This talk will delve into the specific challenges with respect to both design and CAD that is required for these many core chips. The talk will also provide an overview into the market and technology factors guiding and driving this trend. Attendees will be provided with insight into both present and future research vectors to support this nascent exponential.

Keynote 1: Challenges for Electronics Design in the Nano-Scale

Semiconductor technologies exhibited explosive growth in complexity and speed over the last two decades. Since the early 1980s, the device sizes have scaled down from few micrometers to tens of Nano-meters and the operating frequencies have increased from a few megahertz to several gigahertz. Also, the spacing between devices and interconnect have dramatically decreased due to the continuous scaling down of the technology feature size. These trends have led to issues and challenges in the design and analysis of high performance integrated circuits that previous generations did not exhibit. Most of these issues are at the circuit and interconnect (physical) levels. Also, these issues are expected only to increase in importance in future generations of integrated circuits. This talk will overview the most important challenges for electronics design in the nano-scale.

Keynote 2: Low Power Circuit Design Techniques for Nano-scale Era

Power has become the key driving force in processor design as the frequency scale-up is reaching saturation. Technology has seen major shifts from bulk to SOI and then to non-planar devices such as FinFET and Trigates. This talk focuses on technology and important circuit techniques for nanoscale VLSI circuits. Process variability and geometric variation in devices can cause variation in power, reliability which also affects the power-performance envelope. All the key areas of low power optimization such as reduction in active power, leakage power, short circuit power and collision power are power are covered.

Important Weblinks:

1. SoC 2013: http://soc.cs.tut.fi/2013/index.php
2. IEEE FS SP/CAS Chapter: http://www.cs.tut.fi/ieee_spcas/index.htm
3. IEEE Chapter LinkedIn Group: http://www.linkedin.com/groups/IEEE-Finland-Section-SP-CAS-4793814/about?trk=anet_ug_grppro